CLAIMS

What is claimed is:

CLAIM 1

A method for fabricating complementary vertical bipolar junction transistors comprising the steps of:

providing a sapphire substrate;

forming a layer of silicon on said sapphire substrate;

recrystalizing said silicon layer;

forming a P+ region in said silicon layer to become a collector for a PNP transistor;

forming N+ region in said silicon layer to become a subcollector for an NPN transistor;

forming an N silicon layer over said P+ and N+ regions to become an intrinsic base region for said PNP transistor and to become a collector region for said NPN transistor;

forming islands of what is to become said PNP transistor and of what is to become said NPN transistor by removing any silicon therebetween to said sapphire substrate;

forming a P intrinsic base region in said N collector region for said NPN transistor;

forming P+ extrinsic base regions in said P intrinsic base region for said NPN transistor;

forming a P+ emitter region in said N base region for said PNP transistor;

forming an N+ emitter region in said P base region for said NPN transistor;

forming N+ extrinsic base regions in said N base region for said PNP transistor; and

forming individual conducting metal contacts with said emitters and extrinsic bases, said individual conducting metal contacts being formed between oxide regions.

CLAIM 2

The method according to claim 1 wherein said recrystalization is done by a double solid phase epitaxy technique.

CLAIM 3

The method according to claim 1 wherein said silicon layer formed on said sapphire substrate is approximately 0.3 micrometers thick.

CLAIM 4

The method according to claim 1 wherein said N, N+, P and P+ regions are created through ion implantation.

CLAIM 5

The method according to claim 1 wherein said N-type silicon layer is approximately 2.5 micrometers thick.

CLAIM 6

The method according to claim 1 wherein arsenic ion implantation is used to produce said N-type and N+-type regions.

CLAIM 7

The method according to claim 1 wherein boron ion implantation is used to produce said P-type

and P+-type regions.

CLAIM 8

The method of claim 1 further including the steps of:

forming P+ collector plugs in said N base region for said PNP transistor so that said P+ collector plugs are incorporated into said P+ collector for said PNP transistor;

forming N+ collector plug regions in said N collector region for said NPN transistor so that said N+ collector plugs are incorporated into said N+ sub-collector region for said NPN transistor;

forming individual conductive metal contacts with said collector plug regions; and

forming an oxide region between said collector plug metal contacts.

CLAIM 9

The method according to claim 8 wherein said N, N+, P and P+ regions are created through ion implantation.

CLAIM 10

The method according to claim 8 wherein arsenic ion implantation is used to produce said N-type and N+-type regions.

CLAIM 11

The method according to claim 8 wherein boron ion implantation is used to produce said P-type

and P+-type regions.

CLAIM 12

A complementary vertical bipolar junction transistor apparatus comprising:

a sapphire substrate;

a PNP transistor including:

a P+ region formed of an island of recrystalized silicon disposed on said sapphire substrate, said P+ region being a collector region;

an N silicon region disposed within said P+ region, said N silicon region being an intrinsic base region;

a P+ emitter region disposed within said N base region;

N+ extrinsic base regions disposed within said N base region;

individual conducting metal contacts operably coupled to said emitter, said extrinsic base regions and disposed on sidewalls of said collector region; and

an oxide disposed between said conducting metal contacts;

a NPN transistor including:

an N+ region formed of an island of recrystalized silicon disposed on said sapphire substrate and separated from said PNP transistor, said N+ region being a subcollector region;

an N silicon region disposed within said N+ region, said N silicon region being a collector region;

a P intrinsic base region disposed within said N collector region;

an N+ emitter region disposed within said P base region;

forming P+ extrinsic base regions in said P intrinsic base region;

individual conducting metal contacts operably coupled to said emitter, said extrinsic base regions and disposed on sidewalls of said collector region; and

an oxide region disposed between said conducting metal contacts; and

an oxide region disposed on said sapphire substrate between said PNP and NPN transistors.

CLAIM 13

The apparatus according to claim 12 wherein said recrystalization is done by a double solid phase epitaxy technique.

CLAIM 14

The apparatus according to claim 12 wherein said silicon layer on said sapphire substrate is approximately 0.3 micrometers thick.

CLAIM 15

The apparatus according to claim 12 wherein said N, N+, P and P+ regions are created through ion implantation.

CLAIM 16

The apparatus according to claim 12 wherein said N-type silicon layer is approximately 2.5

micrometers thick.

CLAIM 17

The apparatus according to claim 12 wherein arsenic ion implantation is used to produce said N-type and N+type regions.

CLAIM 18

The apparatus according to claim 12 wherein boron ion implantation is used to produce said P-type and P+-type regions.